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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590

04/21/2004

Richard P. Berg, Esq. c/o LADAS & PARRY Suite 2100 5670 Wilshire Boulevard Los Angeles, CA 90036-5679 EXAMINER

COX, CASSANDRA F

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 04/21/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,785	06/19/2003	Jian-Shen Yu	B-5128 621031-0	5987

TITLE OF INVENTION: SEQUENTIAL PULSE TRAIN GENERATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	07/21/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

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If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
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If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.
- □ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
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- III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,785	06/19/2003	Jian-Shen Yu	B-5128 621031-0	5987
7:	590 04/21/2004		EXAMINER	
Richard P. Berg, Esq. c/o LADAS & PARRY			COX, CASSANDRA F	
Suite 2100	KK I		ART UNIT	PAPER NUMBER
	670 Wilshire Boulevard		2816	
Los Angeles, CA 9	0036-5679		DATE MAILED: 04/21/2004	4

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

	Application No.	Applicant(s)	
	Аррисацоп но.	Applicant(s)	
Nation of Allowability	10/600,785	YU, JIAN-SHEN	
Notice of Allowability	Examiner	Art Unit	
· :	Cassandra Cox	2816	
The MAILING DATE of this communicati n appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED or other appropriate comm GHTS. This application is	in this application. If not included nunication will be mailed in due cours	se. THIS
1. This communication is responsive to <u>06/19/03</u> .			
2. The allowed claim(s) is/are <u>1-15</u> .			
3. \boxtimes The drawings filed on <u>19 June 2003</u> are accepted by the E	xaminer.		
 4. Acknowledgment is made of a claim for foreign priority ur a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 		or (f).	
2. ☐ Certified copies of the priority documents have		on No.	
3. ☐ Copies of the certified copies of the priority do	• •		rom the
International Bureau (PCT Rule 17.2(a)).			
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	IENT of this application.		
5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give			JE OF
6. CORRECTED DRAWINGS (as "replacement sheets") mus			
(a) ☐ including changes required by the Notice of Draftspers	on's Patent Drawing Revie	w (PTO-948) attached	
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date			
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment o	or in the Office action of	
Identifying indicia such as the application number (see 37 CFR 1 ach sheet. Replacement sheet(s) should be labeled as such in t			k) of
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.			
Attachment(s)			
1. Notice of References Cited (PTO-892)	5. ☐ Notice of I	nformal Patent Application (PTO-15	2)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)		Summary (PTO-413), ./Mail Date	
3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 06/19/03	98), 7. ⊠ Examiner's	s Amendment/Comment	
4. Examiner's Comment Regarding Requirement for Deposit	_	s Statement of Reasons for Allowand	ce
of Biological Material	9. ☐ Other	THAT THY D CALL AHAN	7
		TIMOTHY P. CALLAHAN SUPERVISORY PATENT EXAMINER	
U.S. Patent and Trademark Office		CALPITACITI LUPITI PARMITELI	

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Richard Berg on 04/09/04.

The application has been amended as follows: On page 6, line 2 "S3" has been replaced with --S4--.

On page 6, line 4 "S3" has been replaced with --S4--.

On page 6, line 28 "output" has been replaced with --input--.

On page 7, line 2 "S4" has been replaced with --S3--.

In line 24 of claim 1, the term "first output" has been replaced with --fifth input--.

In lines 30-31 of claim 1, the term "first output" has been replaced with --fifth input--.

Allowable Subject Matter

- 2. Claims 1-15 are allowed.
- 3. The following is an examiner's statement of reasons for allowance: Claims 1-7 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2a wherein the pulse train generator comprises a first (211) and second (212) dynamic shift register circuit, first (S3), second (S4), third (S1) and fourth (S2) input

Art Unit: 2816

terminal of the first dynamic shift register circuit (211) coupled to receive an initial pulse train (IN), the inverted initial pulse train (IN'), a clock signal (CK) and the inverted clock signal (CK'), the fifth input terminal (S7) of the first dynamic shift register circuit (211) coupled to the first input terminal (S4) of the second dynamic shift register circuit (212), the third (S1) and fourth (S2) input terminal of the second dynamic shift register circuit (212) coupled to receive the inverted clock signal (CK) and the clock signal (CK), respectively; a first (221) and second (222) level shifter, each of which has a first (L1) and second (L2) input terminal, and an output terminal (L3), the first (L1) and second (L2) input terminal of the first level shifter (221) coupled to the first (S5) and second (S6) output terminal of the first dynamic shift register circuit (211), the output terminal (L3) of the first level shifter (221) coupled to the fifth input terminal (S7) of the first dynamic shift register circuit (211), the first (L1) and second (L2) input terminal of the second level shifter (222) coupled to the first (S5) and second (S6) output terminal of the second dynamic shift register circuit (212), the output terminal (L3) of the second level shifter (222) coupled to the fifth input terminal (S7) of the second dynamic shift register circuit (212), respectively; and a first (231) and second (231) inverter having input terminals coupled to the output terminals (L3) of the first (221) and second (222) level shifter, and outputting a first (OUT1) and second (OUT2) sequential pulse train, the output terminal of the first inverter (231) coupled to the second input terminal (S3) of the second dynamic shift register circuit (212) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 8-14 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figures 5a-5b wherein a pulse

Art Unit: 2816

train generator comprises a first (511), second (512) and third (513) dynamic shift register circuit, the first (S4), second (S3) and third (S1) input terminal of the first dynamic shift register circuit (511) coupled to receive an initial pulse train (IN), the inverted initial pulse train (IN') and a clock signal (CK), the fourth input terminal (S2) of the first dynamic shift register circuit (511) coupled to the second input terminal (S4) of the third dynamic shift register circuit (513), the third input terminal (S1) of the second dynamic shift register circuit (512) coupled to receive the inverted clock signal (CK'), the third input terminal (S1) of the third dynamic shift register circuit (513) coupled to receive the clock signal (CK); a first (521), second (522) and third (523) level shifter, the first (L1) and second (L2) input terminal of the first level shifter (521) coupled to the first (S5) and second (S6) output terminal of the first dynamic shift register circuit (511), the first (L1) and second (L2) input terminal of the second level shifter (522) coupled to the first (S5) and second (S6) output terminal of the second dynamic shift register circuit (512), the first (L1) and second (L2) input terminal of the third level shifter (523) coupled to the first (S5) and second (S6) output terminal of the third dynamic shift register circuit (513); and a second (531), third (532), fourth (533), fifth (541), sixth (542), and seventh (543) inverter, input terminals of the second (531), third (532), and fourth (533) inverter coupled to the output terminals (L3) of the first (521), second (522), and third (523) level shifter, output terminals of the second (531) and third (532) inverter coupled to the first input terminals (S3) of the second (512) and third (513) dynamic shift register circuit, input terminals of the fifth (541), sixth (542), and seventh (543) inverter coupled to the output terminals of the second (531), third (532), and fourth (533) inverter, an output

Art Unit: 2816

terminal of the fifth inverter (541) coupled to the second input terminal (S4) of the second dynamic shift register circuit (512), the output terminals of the fifth (541), sixth (542) and seventh (543) inverter outputting a first (OUT1), second (OUT2), and third (OUT3) sequential pulse train, respectively in combination with the rest of the limitations of the base claims and any intervening claims. Claim 15 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figures 5a-5b wherein the pulse train generator comprises a first (511), second (512), and third (513) dynamic shift register circuit, the first (S4) and second (S1) input terminal of the first dynamic shift register circuit (511) coupled to receive an initial pulse train (IN) and a clock signal (CK), the third input terminal (S2)of the first dynamic shift register circuit (511) coupled to the first input terminal (S4) of the third dynamic shift register circuit (513), the second input terminal (S1) of the second dynamic shift register circuit (512) coupled to receive the inverted clock signal (CK'), the second input terminal (S1) of the third dynamic shift register circuit (513) coupled to receive the clock signal (CK); a first (521), second (522), and third (523) level shifter, each of which has a first (L1) and second (L2) input terminal, and an output terminal (L3), the first (L1) and second (L2) input terminal of the first level shifter (521) coupled to the first (S5) and second (S6) output terminal of the first dynamic shift register circuit (511), the first (L1) and second (L2) input terminal of the second level shifter (522) coupled to the first (S5) and second (S6) output terminal of the second dynamic shift register circuit (512), the first (L1) and second (L2) input terminal of the third level shifter (523) coupled to the first (S5) and second (S6) output terminal of the third dynamic shift register circuit (513); and a first (531, 541), second

Art Unit: 2816

(532, 542) and third (533, 543) buffer, input terminals of the first (531, 541), second (532, 542), and third (533, 543) buffer coupled to the output terminals (L3) of the first (521), second (522), and third (523) level shifter, output terminals of the second buffer (532, 542) coupled to the third input terminal (S2) of the first dynamic shift register circuit (511) and to the first input terminal (S4) of the third dynamic shift register circuit (513) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/600,785 Page 7

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

April 13, 2004